**LIBRARY ieee;**

**USE ieee.std\_logic\_1164.all;**

**entity slow\_clock is**

**PORT(**

**clock\_in : in std\_logic;**

**clock\_out : out std\_logic**

**);**

**end slow\_clock;**

**architecture behavior of slow\_clock is**

**signal clock\_tmp : std\_logic;**

**begin**

**process(clock\_in)**

**variable x : integer := 0;**

**begin**

**if(clock\_in'event and clock\_in='0') then**

**x:=x+1;**

**if x = 25000000 then**

**x:=0;**

**clock\_tmp <= not clock\_tmp;**

**clock\_out <= clock\_tmp;**

**end if;**

**end if;**

**end process;**

**end behavior;**